General Description

The MAX5005/MAX5006/MAX5007 are low-dropout (LDO), micropower linear voltage regulators with an integrated microprocessor (μ P) reset circuit for use with USB peripheral devices. Each device is available with a fixed +3.3V output voltage and can deliver up to 150mA load current. Each device features ±15kV transient voltage suppression (TVS) as well as precision 1.5k Ω data-line termination resistors for USB digital signals making them ideal for use with USB peripherals.

The MAX5005/MAX5006/MAX5007 include an internal reset circuit that enables the USB microcontroller 100ms after the LDO regulator output voltage reaches regulation. Reset outputs are available in push-pull (active-low or active-high) and open-drain (active-low) options.

The MAX5005/MAX5006/MAX5007 are optimized for use with a 1 μ F ceramic output capacitor. Each device includes thermal shutdown protection, output short-circuit protection, and output to input reverse leakage protection. These devices also include an active-low manual reset input.

The MAX5005 features an open-drain reset output, the MAX5006 features an active-low push-pull reset output, and the MAX5007 features an active-high push-pull reset output. Each device is available in a space-saving 10-pin μ MAX package.

Applications

USB Peripherals Hand-Held Instruments



_Typical Operating Circuit

____ Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Features

- Integrated ±15kV Transient Voltage Suppressors for D+ and D- Data Lines
- ♦ Pin Selectable Internal D+ and D- Termination Resistors (1.5kΩ ±5%)
- Integrated Microprocessor Reset Circuit with 100ms (min) Timeout
- ♦ 3.3V Output with ±3% Accuracy
- ♦ 25µA Quiescent Current at Full Load
- Small 1µF Output Capacitor
- ♦ Output to Input Reverse Leakage Protection
- Thermal and Short-Circuit Protection
- 10-Pin µMAX Package

Ordering Information

PART	TEMP RANGE	PIN- PACKAGE	RESET OUTPUT
MAX5005_CUB*	0°C to +70°C	10 µMAX	Open- Drain Low
MAX5006_CUB*	0°C to +70°C	10 µMAX	Push-Pull Low
MAX5007_CUB*	0°C to +70°C	10 µMAX	Push-Pull High

*Insert "A" for a 7.5% reset threshold and "B" for a 12.5% reset threshold.



ABSOLUTE MAXIMUM RATINGS

IN to GND	-0.3V to +6V
D+, D- to GND	-0.3V to +6V
MR to GND	0.3V to (V _{OUT} + 0.3V)
RESET, RESET to GND, Push-Pull	0.3V to (V _{OUT} + 0.3V)
RESET to GND, Open-Drain	-0.3V to +6V
OUT, SELR, ENR to GND	0.3V to +6V
Maximum Current to Any Pin	
(except IN, OUT, D+, D-)	± 20mA

Short-Circuit Duration	Indefinite
Continuous Power Dissipation ($T_A = +70^{\circ}C$)	
10-Pin µMAX (derate 5.6mW/°C above +70°C)	444mW
Thermal Resistance (θ_{JA})	180°C/W
Operating Temperature Range	0°C to +70°C
Junction Temperature	+150°C
Storage Temperature Range6	5°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

 $(V_{IN} = +5V, I_{OUT} = 0, C_{OUT} = 2.2\mu$ F, $T_A = 0^{\circ}$ C to +70°C, unless otherwise noted. Typical specifications are at $T_A = +25^{\circ}$ C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	МАХ	UNITS	
Input Voltage Range	VIN	$I_{LOAD} = 100 \text{mA}$	4.0		5.5	V	
Supply Current	IGND	Measured at GND		25	50	μA	
REGULATOR							
Guaranteed Output Current	IOUT		150			mA	
Output Voltage	Vout	$V_{IN} = 4.0V$ to 5.5V, $I_{OUT} = 0$ to 100mA	3.2	3.3	3.4	V	
Dropout Voltago (Noto 2)		$I_{LOAD} = 10 \text{mA}$		20	30	mV	
Dropout voltage (Note 2)	ΔVDO	$I_{LOAD} = 150 \text{mA}$		300	400		
Output Current Limit		$V_{IN} = 5.5V$	165	350		mA	
Input Reverse Leakage Current		$V_{IN} = 0, V_{OUT} = 5.5V$		1		μA	
Startup Response Time		Rising edge of V _{IN} to V _{OUT} $R_L = 500 \Omega$		500		μs	
Thermal Shutdown Temperature	TJSHDN			160		°C	
Thermal Shutdown Hysteresis	Δ T _J SHDN			20		°C	
RESET CIRCUIT							
Poset Threshold (Note 3)	\/ _	MAX500_ACUB	2.92	3.05	3.18	V	
heset miesiola (Note 3)	VIH	MAX500_BCUB	2.75	2.89	3.01		
Reset Timeout Period	t _{RP}		100	200	300	ms	
V _{OUT} to Reset Delay	t _{RD}			75		μs	
MR Input Voltage	VIL				0.2 x Vout	V	
	VIH		0.8 x V _{OUT}				
MR Minimum Input Pulse Width			1			μs	
MR Glitch Rejection				120		ns	
MR to Reset Delay				500		ns	
MR Pullup Resistance to OUT			10	25	45	kΩ	
SELR Input Voltage	VIL	Connects RTERM to D-			0.2 x V _{OUT}	V	
	VIH	Connects R _{TERM} to D+	0.8 x V _{OUT}			v	

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{IN} = +5V, I_{OUT} = 0, C_{OUT} = 2.2\mu$ F, $T_A = 0^{\circ}$ C to $+70^{\circ}$ C, unless otherwise noted. Typical specifications are at $T_A = +25^{\circ}$ C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	ТҮР	MAX	UNITS	
SELR Input Current		SELR = GND or OUT		-1		1	μA	
	VIL	R _{TERM} enabled				0.2 x V _{OUT}	- V	
ENR Input voltage	VIH	R _{TERM} disabled		0.8 x Vout				
ENR Input Current		$\overline{\text{ENR}}$ = GND or OUT		-1		1	μA	
Open-Drain RESET Output Low	Vo	$V_{OUT} \ge 1.0V$, $I_{SINK} = 50\mu A$, reset asserted				0.3	V	
Voltage (MAX5005)	VOL	$V_{OUT} \ge 2.7V$, $I_{SINK} = 3.2mA$, reset asserted				0.4		
Open-Drain Reset Output Leakage Current (MAX5005)	I _{LKG}	Reset not asserted		-1.0		1.0	μΑ	
		$V_{OUT} = 1.0V$, $I_{SINK} = 50\mu A$, reset asserted				0.3		
Push-Pull RESET Output Voltage (MAX5006)	V _{OL}	V _{OUT} > V _{TH(MIN)} , I _{SINK} = 3 asserted	8.2mA, reset			0.4	V	
	V _{OH}	VOUT > VTH(MAX), ISOURCE reset not asserted	= 500μΑ,	0.8 x Vout				
Push-Pull RESET Output Voltage (MAX5007)	V _{OL}	$V_{OUT} > V_{TH(MAX)}, I_{SINK} = 3.2mA,$ reset not asserted $V_{OUT} = 1.0V, I_{SOURCE} = 150\muA, reset$ asserted				0.4	- V	
	Voh			0.8 x Vout				
USB OPTIONS AND TRANSIENT	SUPPRESS	SION						
D+/D- R _{TERM} Impedance		$\overline{\text{ENR}}$ = GND, SELR = GND	or OUT	1425	1500	1575	Ω	
D+/D- Input Leakage Current		$V_{\overline{\text{ENR}}} = V_{OUT} = 3.3V$		-1		1	μA	
		1MHz, 100mVp-p signal	$\overline{\text{ENR}} = \text{OUT}$		5.5		_	
D+ to D- Capacitance		applied at D+ and D-, V _{OUT} = 3.3V	Unpowered		24		рF	
		1MHz, 100mVp-p signal	$\overline{\text{ENR}} = \text{OUT}$		40			
D+, D- Capacitance to GND		applied at D+ and D-, V _{OUT} = 3.3V	Unpowered		47		pF	
ESD Trigger Voltage		dV/dt \leq 1V/ns, V _{D+} or V _{D-} :	> 3.6V	3.6	5		V	
Surge Trigger Voltage		$dV/dt \le 2V/\mu s$, V_{D+} or $V_{D-} > 3.6V$		3.6	16		V	
Clamping Voltage		6A, pulse width = 200ns to 40μ s			16		V	
Surge Current 16V, pulse w		16V, pulse width = 200ns to	o 40µs		±6		Α	
		Human Body Model MIL-STD-883			±16			
D+/D- to GND ESD		Contact Discharge IEC1000-4-2 (EN61000-4-2)		±8 ±15		kV		
		Air Discharge IEC1000-4-2 (EN61000-4-2)						

Note 1: All devices are 100% tested at T_A = +25°C. Limits over temperature are guaranteed by characterization and not production tested.

Note 2: Dropout voltage is defined as V_{IN} - V_{OUT} when V_{OUT} is 2% below the value of V_{OUT} for $V_{IN} = V_{OUT} + 1V$.

Note 3: Specification is guaranteed to $\pm 4\sigma$ limit.

 $(V_{IN} = +5V, I_{OUT} = 0, C_{OUT} = 2.2\mu F$, unless otherwise noted.)

Typical Operating Characteristics



MAX5005/MAX5006/MAX5007

Typical Operating Characteristics (continued)

 $(V_{IN} = +5V, I_{OUT} = 0, C_{OUT} = 2.2\mu$ F, unless otherwise noted.)









1.0ms/div



Pin Description

PIN	NAME	DESCRIPTION
1	IN	Regulator Input. Supply voltage ranges from +4.0V to +5.5V. Bypass with a 1 μ F ceramic capacitor to ground.
2	D+	D+ ESD/Transient Suppression Input. Connect directly to USB port D+ data input. SELR high and $\overline{\text{ENR}}$ low connects D+ to OUT through a 1.5k Ω resistor.
3, 9	GND	Ground. This pin also functions as a heatsink. Solder to large pads or the circuit board ground plane to maximize thermal dissipation.
4	D-	D- ESD/Transient Suppression Input. Connect directly to USB port D- data input. SELR low and $\overline{\text{ENR}}$ low connects D- to OUT through a 1.5k Ω resistor.
5	SELR	USB Full-Speed/Low-Speed Termination Resistor Select. Logic high connects the termination resistor to D+ for full-speed peripherals. Logic low connects the termination resistor to D- for low-speed peripherals. An internal $1.5 k\Omega$ resistor connects to OUT when $\overline{\text{ENR}}$ is low.
6	ENR	USB Termination Resistor Enable. When reset is not asserted, $\overline{\text{ENR}}$ low enables the termination resistor connection. $\overline{\text{ENR}}$ high or a reset disables the termination resistor connection.
7	RESET	Active-Low Reset Output. RESET remains low while V_{OUT} is below the reset threshold or while \overline{MR} is held low. RESET remains low for the duration of the reset timeout period after the reset conditions are terminated. (MAX5005/MAX5006 ONLY)
/	RESET	Active-High Reset Output. RESET remains high while V_{OUT} is below the reset threshold or while \overline{MR} is held low. RESET remains high for the duration of the reset timeout period after the reset conditions are terminated. (MAX5007 ONLY)
8	MR	Active-Low Manual Reset Input. A logic low forces a reset. Reset remains asserted for the duration of the reset timeout period after $\overline{\text{MR}}$ transitions from low to high. Leave unconnected or connect to OUT if not used. $\overline{\text{MR}}$ has an internal pullup resistor of 25k Ω to OUT.
10	OUT	Voltage Regulator Output. Fixed +3.3V. Sources up to 150mA. Bypass with a 1μ F (min) capacitor for full rated performance.



Figure 1. Functional Diagram

Detailed Description

The MAX5005/MAX5006/MAX5007 are USB application-specific, low-dropout, low-quiescent current linear regulators with an integrated μ P reset circuit (see Figure 1). The devices drive loads up to 150mA and are available with a fixed output voltage of +3.3V. Features include 1.5k Ω D+ and D- termination resistors and ±15kV transient voltage suppression (TVS) in accordance with IEC1000-4-2 (EN61000-4-2) Air Discharge Method and MILSTD883C- Method 3015-6 making the MAX5005/MAX5006/MAX5007 ideal for use with USB peripheral devices. The internal reset circuit monitors the regulator output voltage and asserts a reset signal when the output is typically -7.5% out of regulation for MAX500_BCUB.

Reset Circuit

The reset supervisor circuit is fully integrated in the MAX5005/MAX5006/MAX5007, and uses the same reference voltage as the regulator. Two supply tolerance reset thresholds, typically -7.5% and -12.5%, are available for each type of device.

7.5% reset: Reset does not assert until the regulator output voltage is at least -3.6% out of tolerance and always asserts before the regulator output voltage is -11.5% out of tolerance.

12.5% reset: Reset does not assert until the regulator output voltage is at least -8.8% out of tolerance and always asserts before the regulator output voltage is -16.7% out of tolerance.

Reset Output

The MAX5005/MAX5006/MAX5007 μP supervisory circuits assert a reset during power-up, power-down, and



brownout conditions. Reset is guaranteed to be logic high or low depending on the device chosen (see *Ordering Information*). RESET or RESET asserts when V_{OUT} is below the reset threshold and remains asserted for at least 100ms minimum after V_{OUT} rises above the reset threshold. RESET or RESET also asserts when MR is pulled low.

SELR and ENR When reset is not asserted a logic high to SELR connects a $1.5k\Omega$ termination resistor from D+ to OUT for full speed USB peripherals and a logic low connects a $1.5k\Omega$ termination resistor from D- to OUT for low-speed peripherals. Logic low on ENR enables the selected termination resistor connection and logic high disables the selected termination resistor connection. An asserted reset always disconnects the termination resistors.

D+ and D-

D+ and D- include transient voltage suppressors rated at ± 15 kV (see USB ± 15 kV Transient Voltage Suppression section).

The proprietary TVS shunt circuit passes no data through the MAX5005/MAX5006/MAX5007, thereby eliminating delays associated with series protection circuits. D+ and D- have only 1μ A of leakage current and a typical input capacitance of 40pF at 1MHz.

Manual Reset Input

Many μ P-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic low on $\overline{\text{MR}}$ asserts a reset while the regulator output voltage is still within tolerance.

Reset remains asserted while $\overline{\text{MR}}$ is low and for the reset timeout period (100ms minimum) after $\overline{\text{MR}}$ returns high. The $\overline{\text{MR}}$ input has an internal pullup of $25 \text{k}\Omega$ (typ) to OUT. Drive this input with TTL/CMOS logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{\text{MR}}$ to GND to create a manual reset function; external debounce circuitry is not required. If $\overline{\text{MR}}$ is driven from long cables or the device is used in a noisy environment, connect a 0.1µF capacitor from $\overline{\text{MR}}$ to GND to provide additional noise immunity. For proper operation, ensure that the voltage on $\overline{\text{MR}}$ is not greater than a diode drop above V_{OUT}.

Output to Input Reverse Leakage Protection

An internal circuit monitors the input and output voltages. When the output voltage is greater than the input voltage, the internal pass transistor and parasitic diodes turn off, and OUT powers the device. There is no leakage path from OUT to IN. Therefore, the output can be powered from an auxiliary supply such as a backup battery without any need for additional blocking diodes.

Current Limit

The MAX5005/MAX5006/MAX5007 include a current limiter that monitors and controls the pass transistor's gate voltage, limiting the output current to 350mA (typ). For design purposes, consider the current limit to be 160mA (min) to 600mA (max). The output can be shorted to ground for an indefinite period without damaging the part.

Thermal Protection

When the junction temperature exceeds $T_J = +160^{\circ}C$, an internal thermal sensor signals the shutdown logic, turning off the pass transistor and allowing the IC to cool. The thermal sensor turns the pass transistor on again after the IC's junction temperature decreases by 20°C, resulting in a pulsed output during continuous thermal overload conditions. Thermal overload protection is designed to protect the MAX5005/MAX5006/MAX5007 in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of $T_J = +150^{\circ}C$.

Operating Region and Power Dissipation The MAX5005/MAX5006/MAX5007's maximum power dissipation depends on the thermal resistance of the case and circuit board, the temperature difference between the die junction and the ambient air, and the rate of airflow. The power dissipation across the device is $P = I_{OUT}$ (V_{IN} - V_{OUT}). The maximum power dissipation is:

$\mathsf{P}_{\mathsf{MAX}} = (\mathsf{T}_{\mathsf{J}} - \mathsf{T}_{\mathsf{A}}) / (\Theta_{\mathsf{JA}})$

where $T_J - T_A$ is the temperature difference between the die junction and the surrounding air, Θ_{JA} is the thermal resistance of the package from junction to ambient.

The MAX5005/MAX5006/MAX5007's ground pin (GND) performs the dual function of providing an electrical connection to the system ground and channeling heat away. Connect GND to the system ground using a large pad or ground plane. For optimum performance, minimize trace inductance to D+, D-, and GND.

Applications Information

Capacitor Selection and Regulator Stability

For stable operation over the full temperature range and with load currents up to 150mA, use a 1μ F (min) output capacitor. To reduce noise and improve load transient response, stability, and power-supply rejection, use large output capacitor values such as 10μ F.



Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature. With dielectrics such as Z5U and Y5V, it may be necessary to use 2.2µF or more to ensure stability at temperatures below -10°C. With X7R or X5R dielectrics, 1µF should be sufficient at all operating temperatures. Also, for high-ESR tantalum capacitors, 2.2µF or more may be needed to maintain stability. A graph of the Region of Stable COUT ESR vs. Load Current is shown in the *Typical Operating Characteristics*.

To improve power-supply rejection and transient response use a 1μ F capacitor between IN and GND.

Negative-Going VOUT Transients

These devices are relatively immune to short-duration, negative-going VOUT transients. The Typical Operating Characteristics section shows a graph of the Maximum Pulse Duration vs. Reset Threshold Overdrive for which reset is not asserted. The graph was produced using negative going output transients starting at VOUT and ending below the reset threshold by the magnitude indicated (Reset Threshold Overdrive). The graph shows the maximum pulse width that a negative going Vout transient can typically have without triggering a reset pulse. As the amplitude of the transient increases (i.e., goes further below the reset threshold), the maximum allowable pulse width decreases. Typically, a VOUT transient that goes only 10mV below the reset threshold and lasts for 75µs will not trigger a reset pulse.

USB ±15kV Transient Voltage Suppression

The universal serial bus (USB) simplifies interconnectivity between peripheral devices and personal computers. USBs offer high-speed data communication rates (up to 12Mbps) using only two lines (D+ and D-). CMOS based USB peripherals that utilize deep submicron technologies are more susceptible to electrostatic discharge (ESD) failure due to shorter channel lengths, shallower drain/source junctions, and lightly doped drain structures. The MAX5005/MAX5006/MAX5007 incorporate a proprietary transient voltage suppression (TVS) circuit for use with submicron devices.

The TVS design complies with IEC-1000-4-2 level 4 (EN61000-4-2) \pm 15kV Air Discharge and \pm 8kV Contact Discharge as well as MIL STD 883C-Method 3015-6 level 3.

The TVS circuit handles up to 11A of surge current. The TVS/ESD structure is directly coupled to the output of the LDO regulator.

TVS Surge Test Information

Figure 2 shows the test circuit used to generate the 8/40µs short circuit waveform of Figure 3. Figures 4, 5, and 6 show the actual surge current I/V characteristics with various capacitive loads.

ESD Performance

The MAX5005/MAX5006/MAX5007 are characterized to the following limits on D+, D-, and IN:

- ±15kV using the Human Body Model
- ±8kV using the Contact Discharge Method specified in IEC 1000-4-2 (EN61000-4-2)
- ±15kV using the Air-Gap Discharge Method specified in IEC 1000-4-2 (EN61000-4-2).

Note that in order to achieve the above ESD levels on IN, a ceramic $1\mu F$ ceramic capacitor should be connected from IN to GND.

ESD Test Conditions

ESD performance depends on several conditions. Contact Maxim for a reliability report that documents test setup, methodology, and results.

Human Body Model

Figure 7 shows the Human Body Model, and Figure 8 shows the current waveform it generates when discharged into low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a $1.5 \mathrm{k}\Omega$ resistor.

ESD Transmission Line Pulsing

Figure 9 shows the test circuit used for transmission line pulsing conditions. The 200ns pulsewidth has a rise time of 4ns. Figure 10 shows the Current vs. Voltage characteristics for various output capacitance values.



Figure 2. Surge Current Test Circut



Figure 4. Surge Current I/V Characteristic ($C_{OUT} = 0$)



Figure 6. Surge Current I/V Characteristic ($C_{OUT} = 10\mu F$)



Figure 3. Test Circuit Surge Current Waveform (Short-Circuit Load)



Figure 5. Surge Current I/V Characteristic ($C_{OUT} = 1\mu F$)



Figure 7. Human Body ESD Test Model



Figure 9. Transmission Line Pulsing Setup for ESD I/V Characteristics



Figure 8. Human Body Model Current Waveform



Figure 10. Transmission Line Pulsing I/V Characteristic $(C_{OUT} = 0)$



Figure 11. Transmission Line Pulsing I/V Characteristic ($C_{OUT} = 1\mu F$)





Figure 12. Transmission Line Pulsing I/V Characteristic ($C_{OUT} = 10 \mu F$)

Chip Information

TRANSISTOR COUNT: 890 PROCESS: BICMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



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